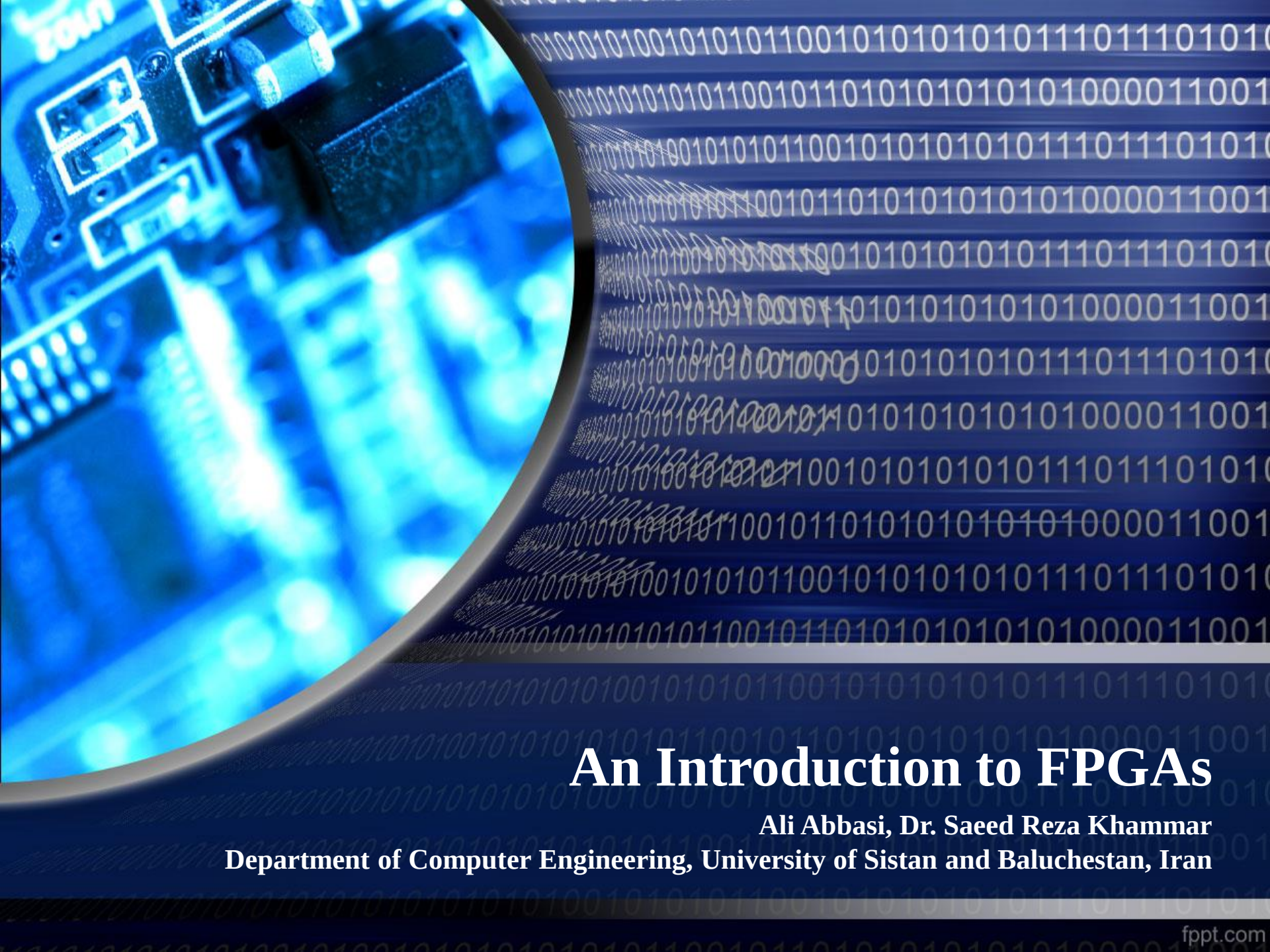

An Introduction to FPGAs

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fppt.com

Chapter 4: Introduction to FPGAs

- FPGA Structure
- CLB Structure
- Application Specific Blocks in FPGA
- FPLD Programming Technologies
- FPGA Market and Examples
- Design Flow

FPGA Structure

- **Configurable Logic Blocks:**

Also known as Logic Block(CB), Logic Cell(LC),...

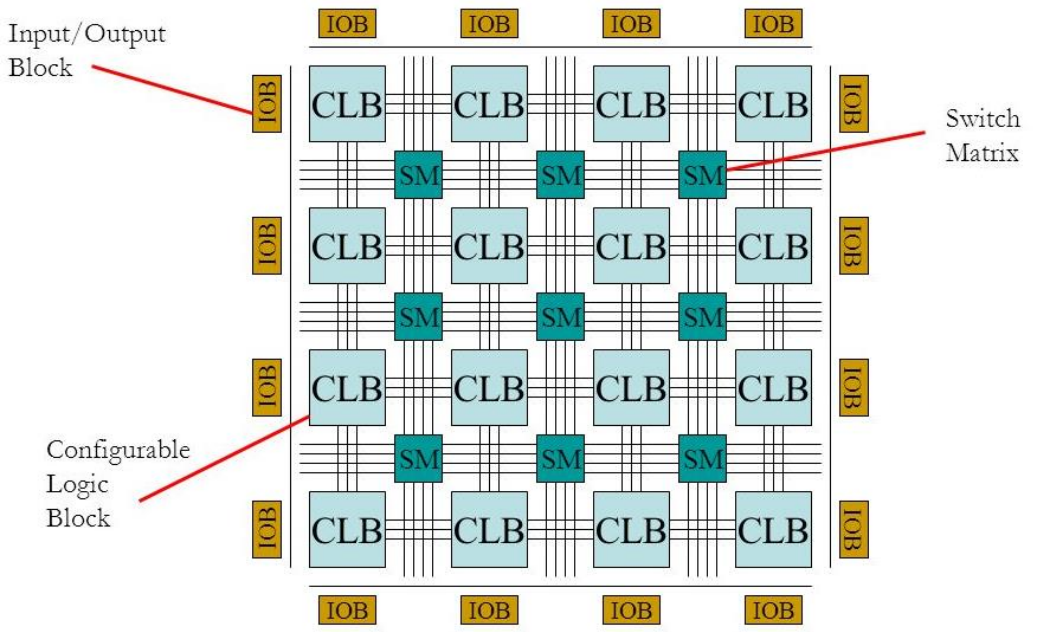
Programmable blocks to perform logic functions

- **Switch Matrix:**

Programmable switches to establish connection between CLBs and I/O Blocks.

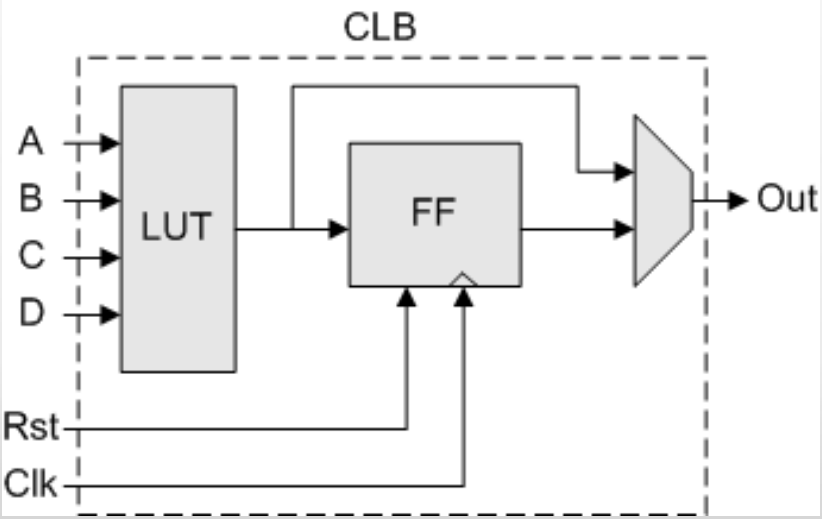
- **Input/Output Blocks:**

An interface for external connections to FPGA



CLB Structure

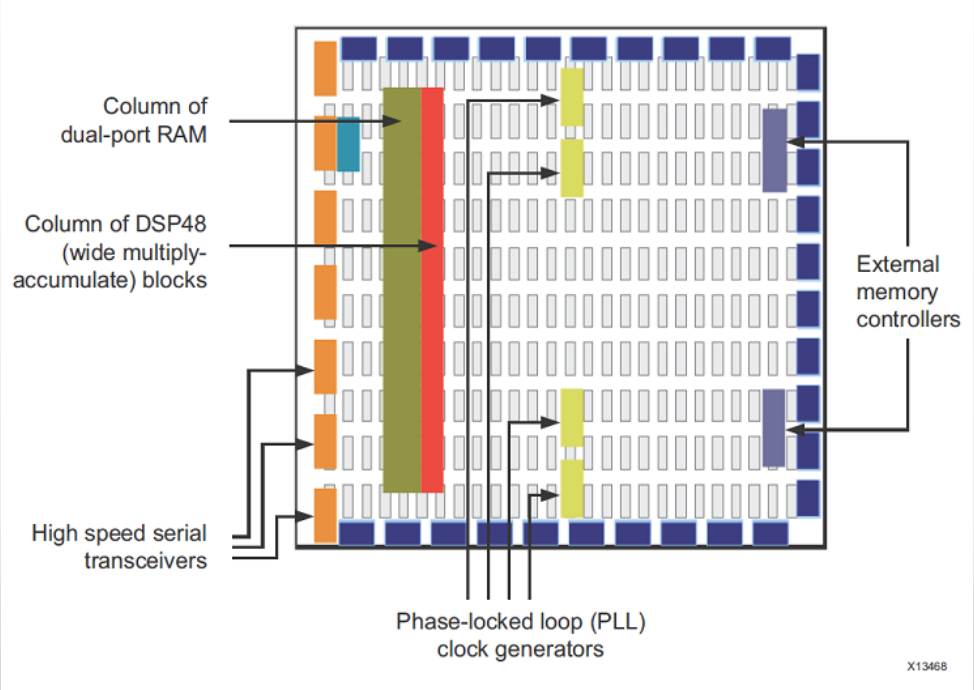
- Each CLB is a PLD-like block.
- Plus some usefull elements like Flip-Flops.
- CLB architecture and design of each FPGA is exclusive (see data-sheets for more information about blocks).
- They commonly use SoP-based, LUTs, or multiplexers for programmable logic implementation *.



* See Chapter 3, Programmable Logic Basis.

Application Specific Blocks in FPGAs

- There are some pre-manufactured full-custom blocks instead of CLBs.
- These blocks are designed to perform an specific task.
- Examples: Memory Blocks, Processor Blocks, Arithmetic Blocks, Clock Management Blocks, Gigabit Transceiver Blocks

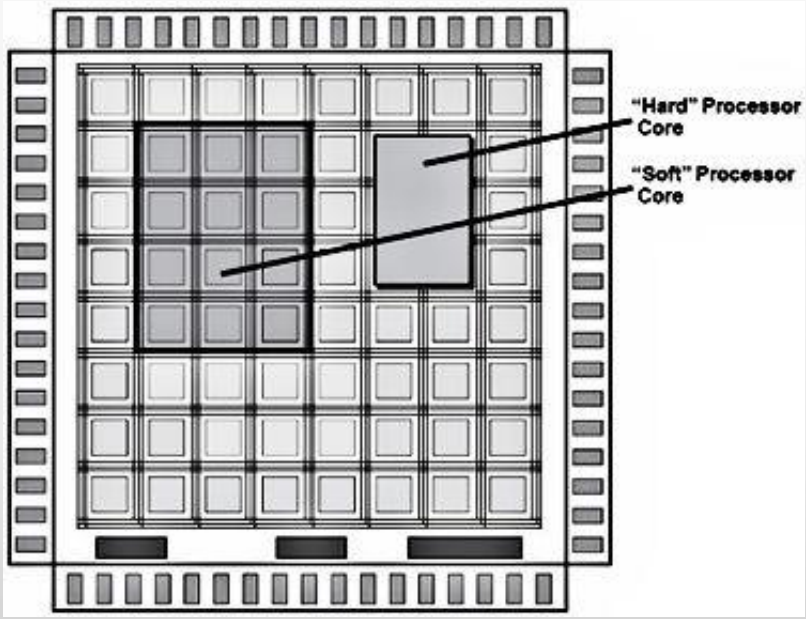


Memory Blocks

- There are two types of memory in FPGAs:
  - Blocked Memory
  - Distributed Memory
- Blocked memories are desgined full-custom in companies and are ready to be used by designers.
- Also, designers can use CLBs for implementing a memory (not sufficient enough, but useful) which is called a distibuted memory.

Processor Blocks

- A specific block to implement an Instruction Set Architecture (ISA) beside usual digital designs.
- FPGA manufacturers define the instruction set.
- Each company has its own ISA (e.g. Microblaze for Xilinx, Nios II for Intel).
- Despite these hard processor cores, designers can implement their own processor using CLBs (also known as a soft processor).

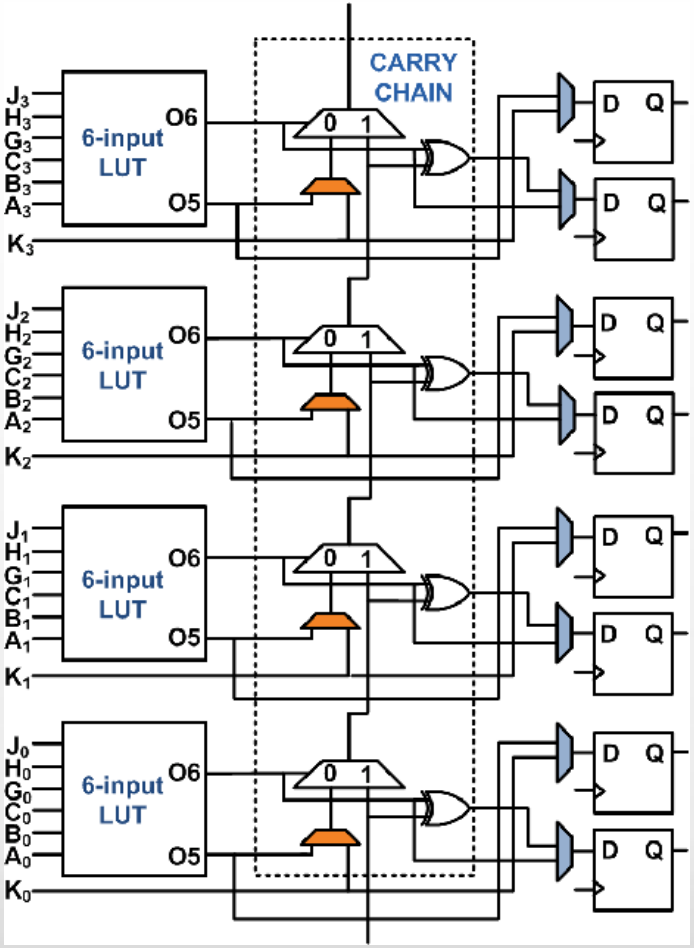


Arithmetic Blocks

- Implementing multipliers using CLBs needs a lot of recources and it will have a slow operation. Therefore, hard design of these blocks in FPGAs helps designers with better recource allocation.

- Performing large-sized sum or sub needs a large carry chain. Routing these carries using SBs will remarkably reduces the performance, so there are some direct connections between adjacent CLBs.

- The main use of these blocks is in digital signal processing (DSP) that needs a lot of arithmetic operations.

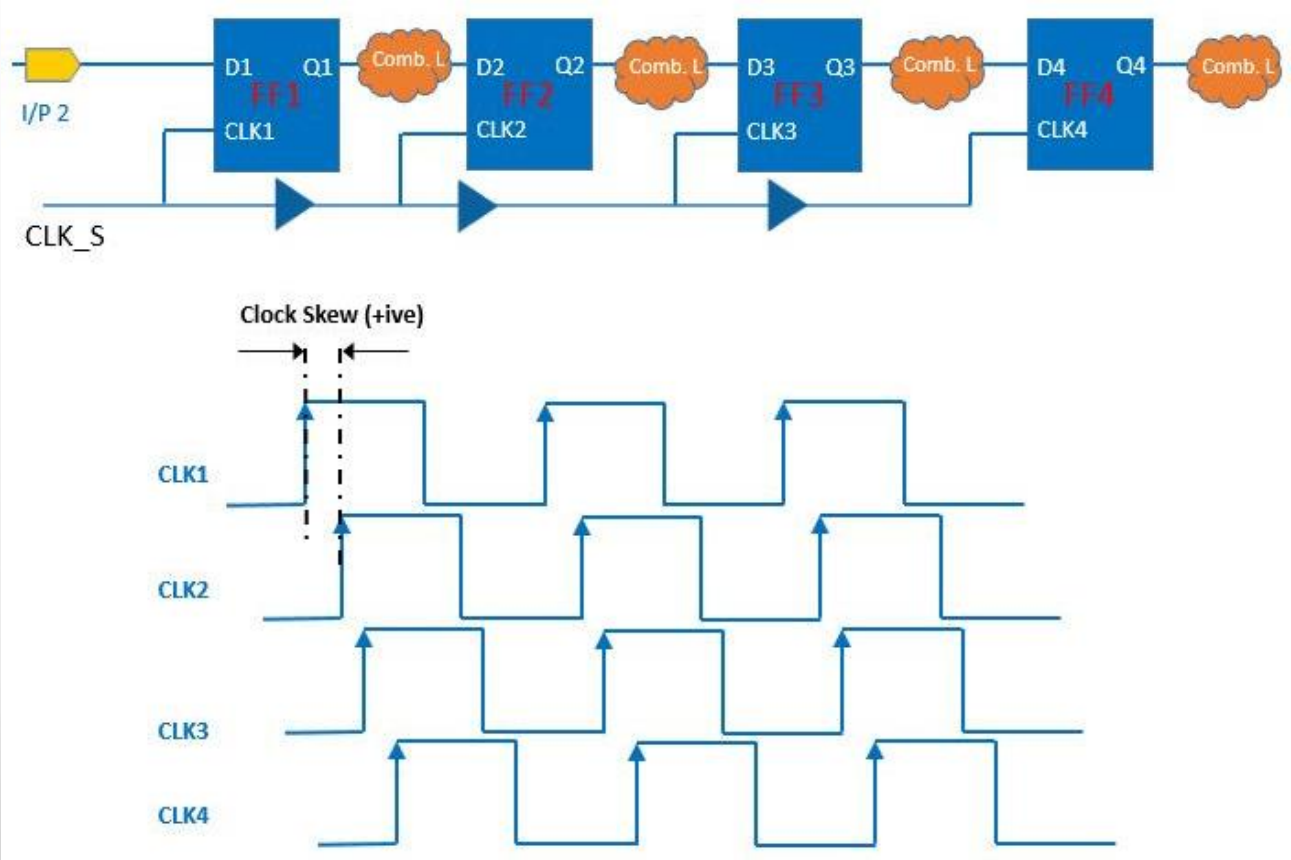


Clock Management Blocks

- Clock problems acccure due to noise or weakening over distance.
  - Clock Skew
  - Jitter

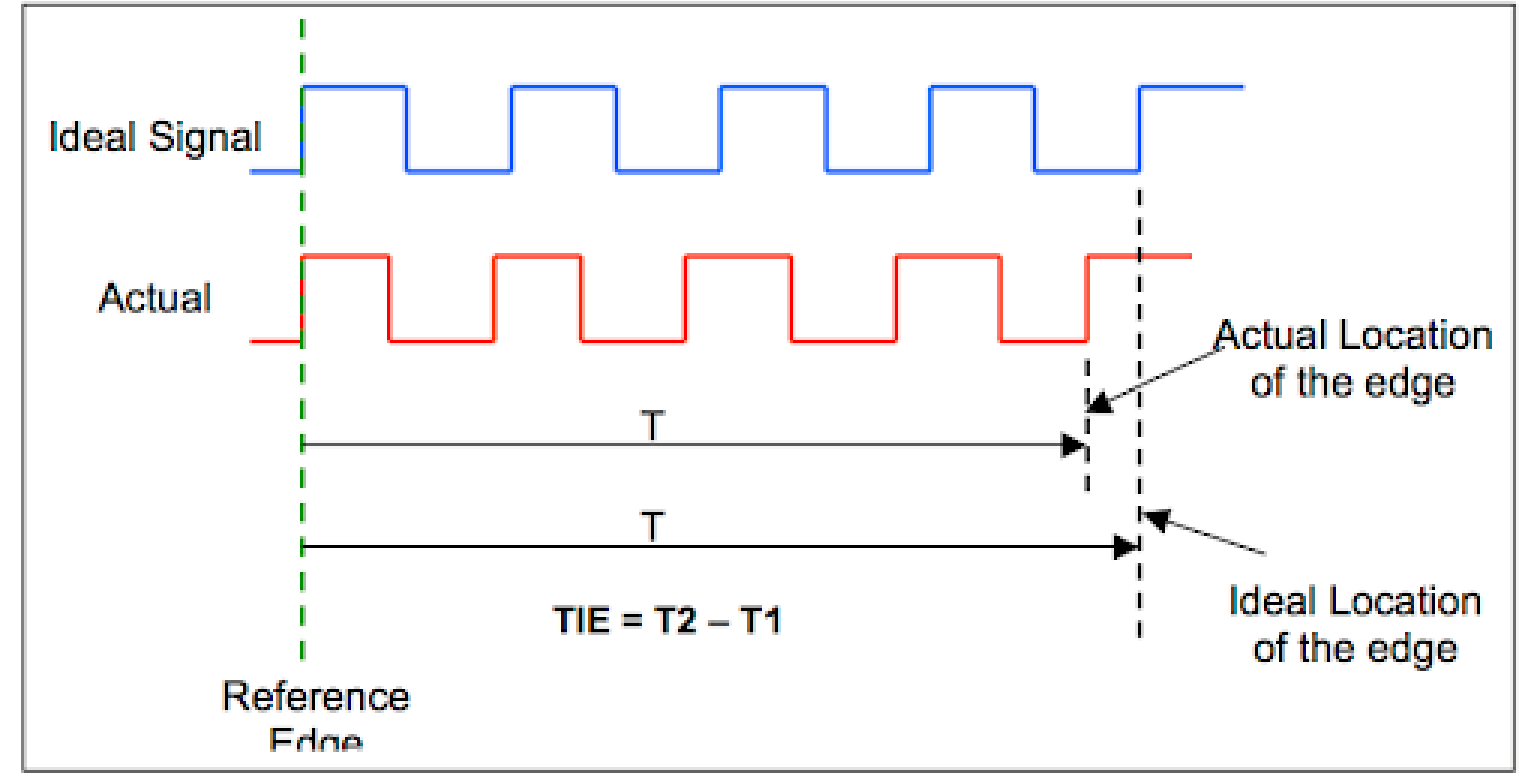
Clock Skew

- A phenomenon in synchronous digital circuit systems in which the same sourced clock signal arrives at different components at different times.



Jitter

- Deviation from true periodicity of a presumably periodic signal (e.g. clock signal)



Clock Management Blocks (cont.)

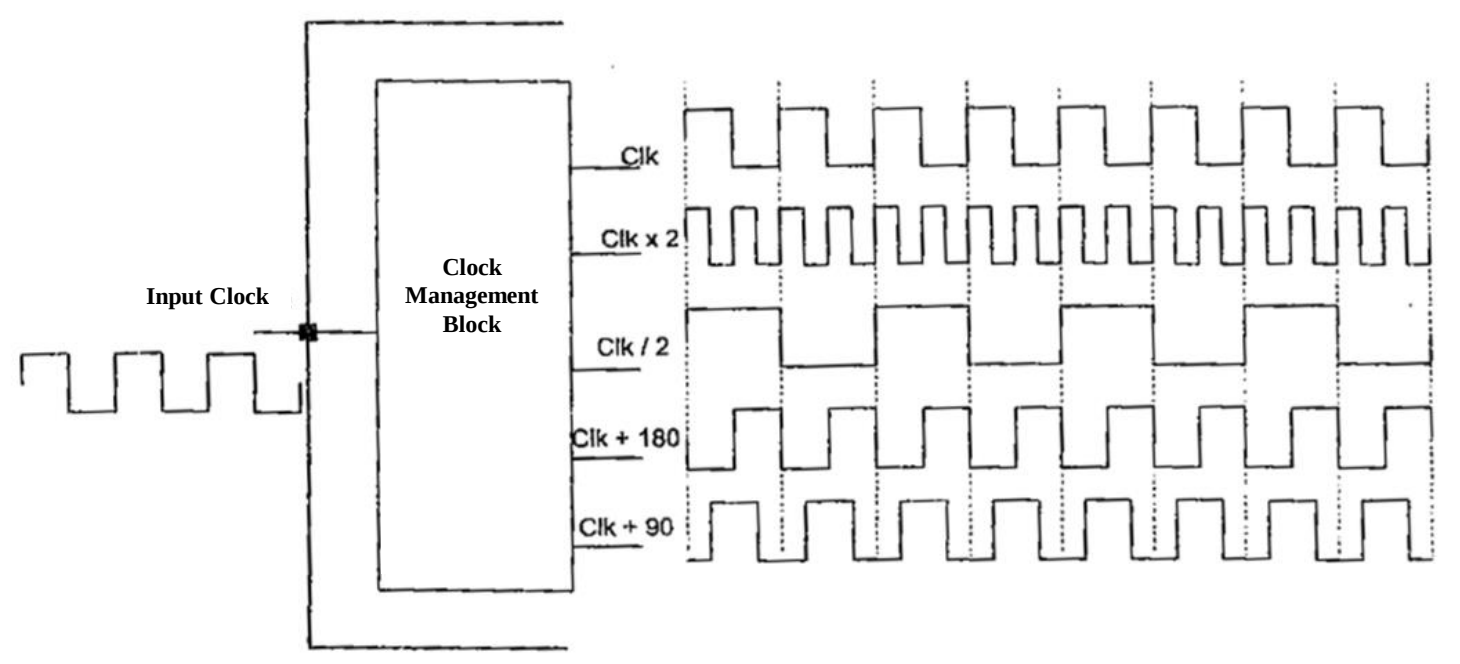
- Clock problems acccure due to noise or weakening over distance.
  - Clock Skew
  - Jitter

- Clock management block overcomes clock skew by monitoring signals with skew (as feedback) and changing the phase of the source clock until the skew fades.

- Also, it solves the jitter problem.

Clock Management Blocks (cont.)

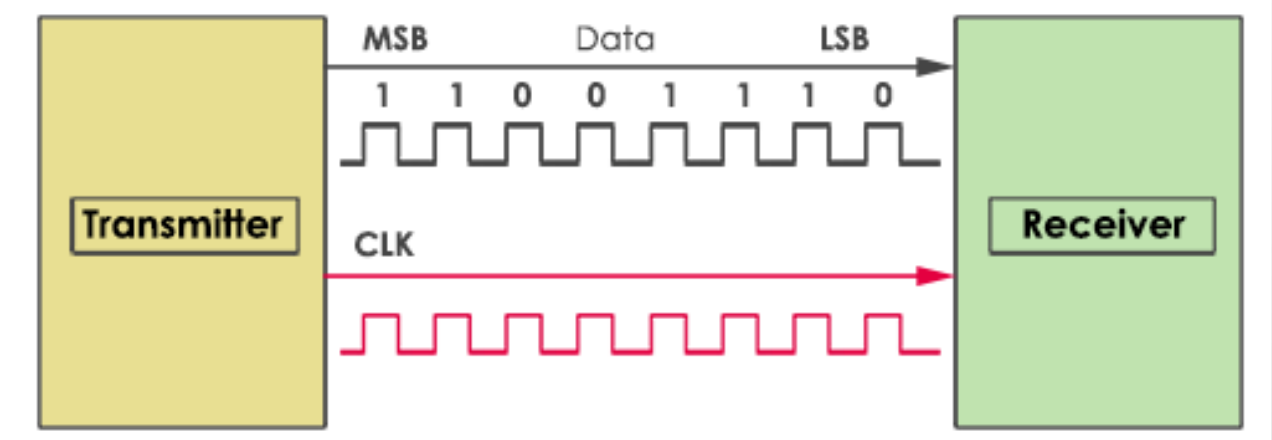
- Since FPGAs recieve only one clock from external sources (e.g. an oscillator), one of the other important functions of a clock management block is to generate clock signals with different frequencies from the source clock (designers control the frequency ratio and phase difference).



Picture Source: Computer-Aided Digital Systems Design, Dr Morteza Seheb Zamani, page 125, with modifications

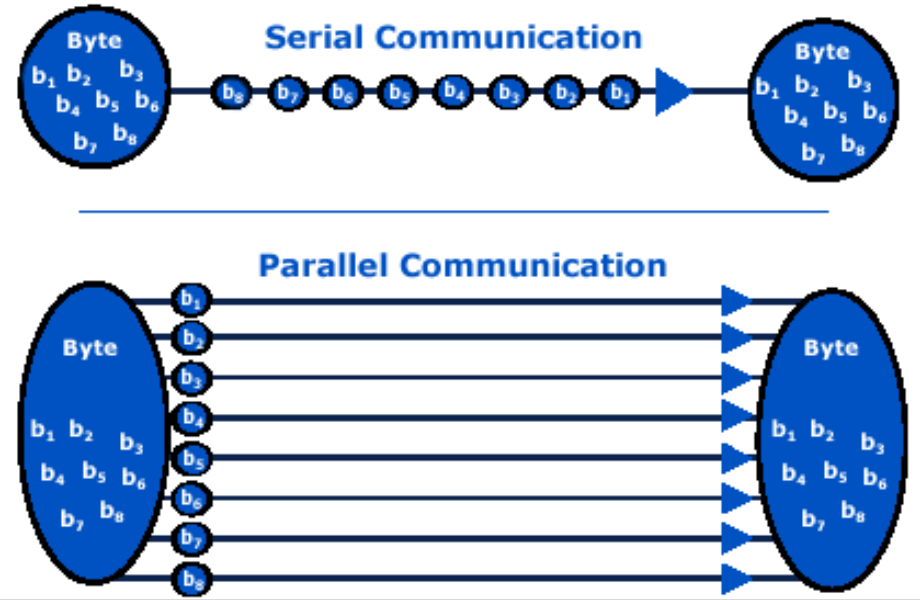
Gigabit Transceiver Blocks

- Can be considered as an I/O block.
- But supports high-speed data transmission (~Gbps)
- Transmits bits in serial (one bit per cycle – single-ended or differential)



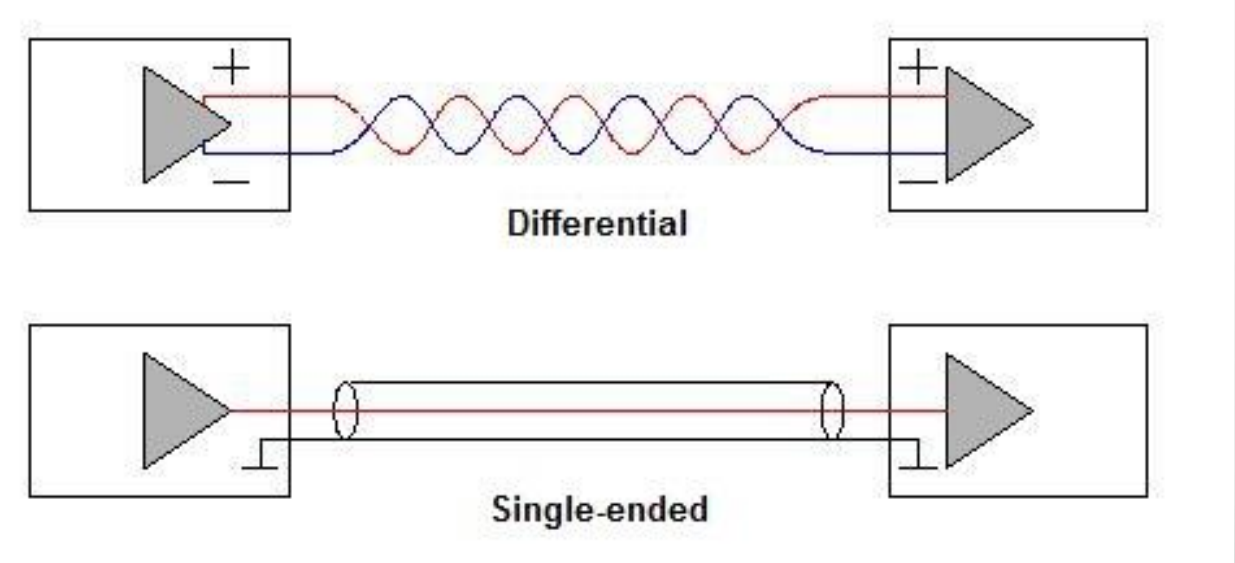
Gigabit Transceiver Blocks (cont.)

- Much better than parallel data communication (e.g. use of 64 I/O pins for 64 bits of data?)
- What about electromagnetic effect on these 64 wires
- Synchronization of these 64 connections with one clock is much challenging

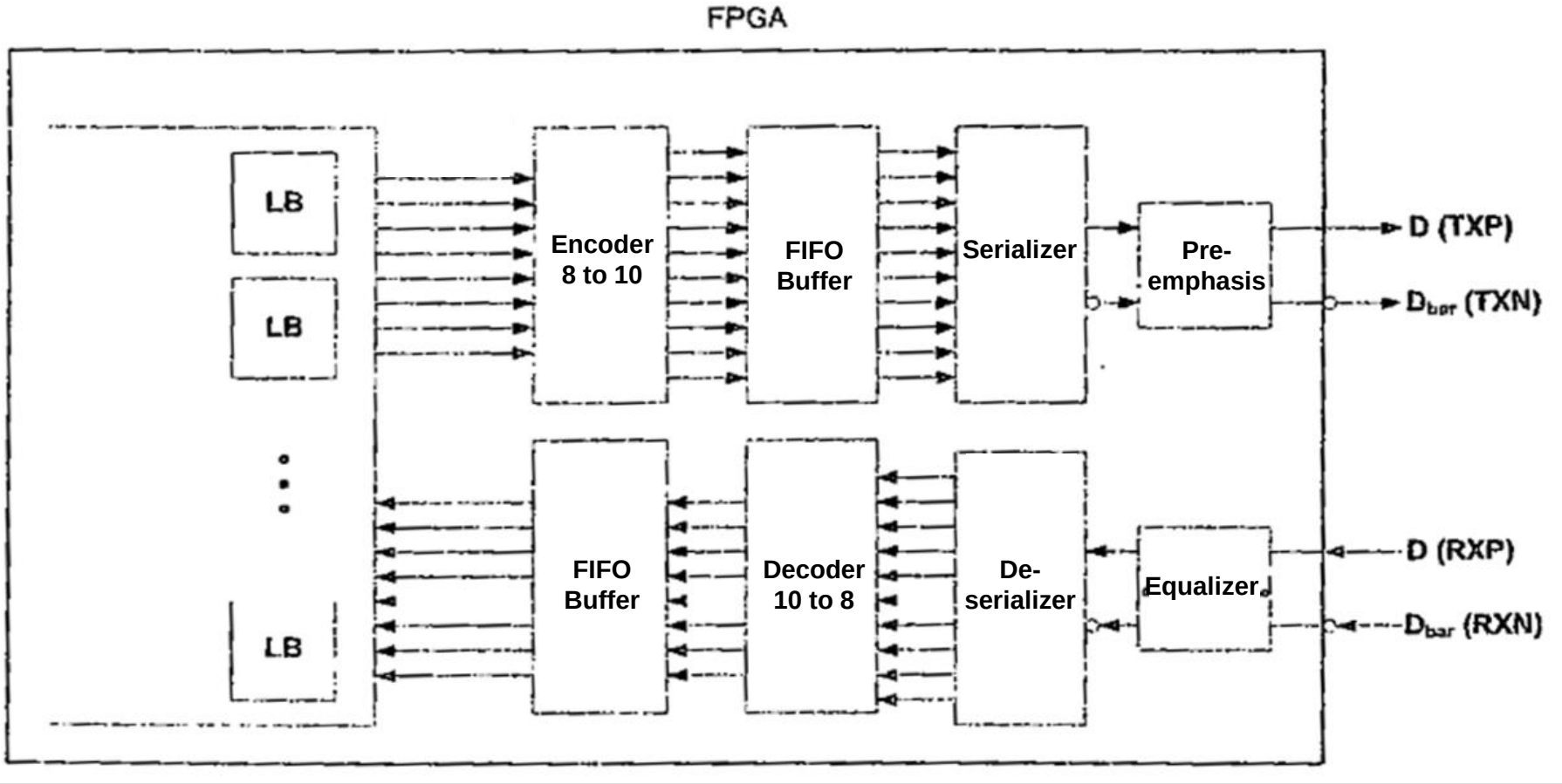


Single-ended vs Differential

- Both refer to the reference for a voltage
- Single-ended is referred to ground while differential is referred to some other voltage



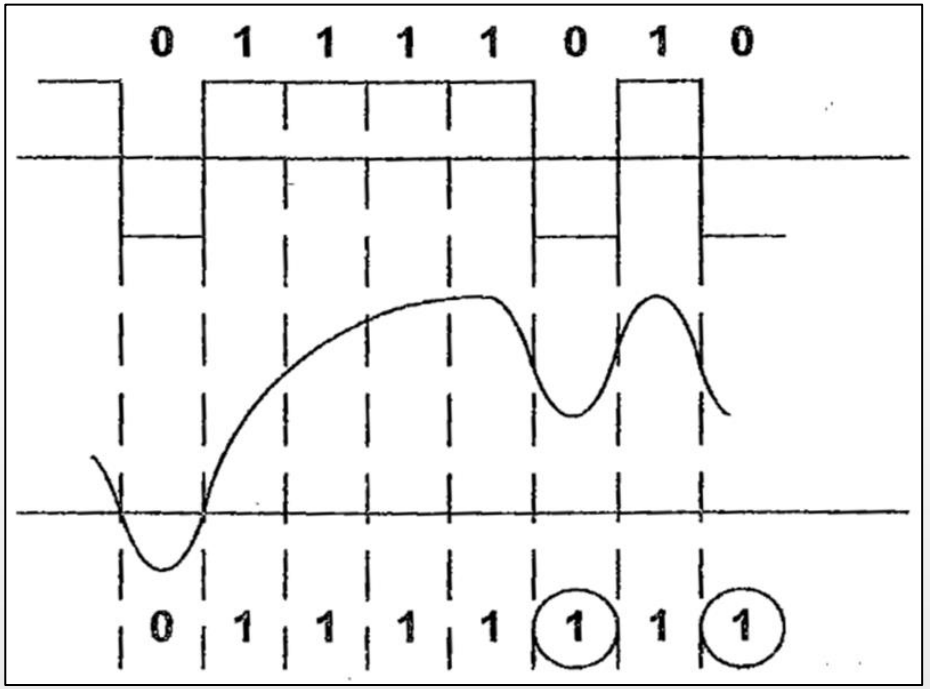
Gigabit Transceiver Blocks Structure



Picture Source: Computer-Aided Digital Systems Design, Dr Morteza Seheb Zamani, page 92, with modifications

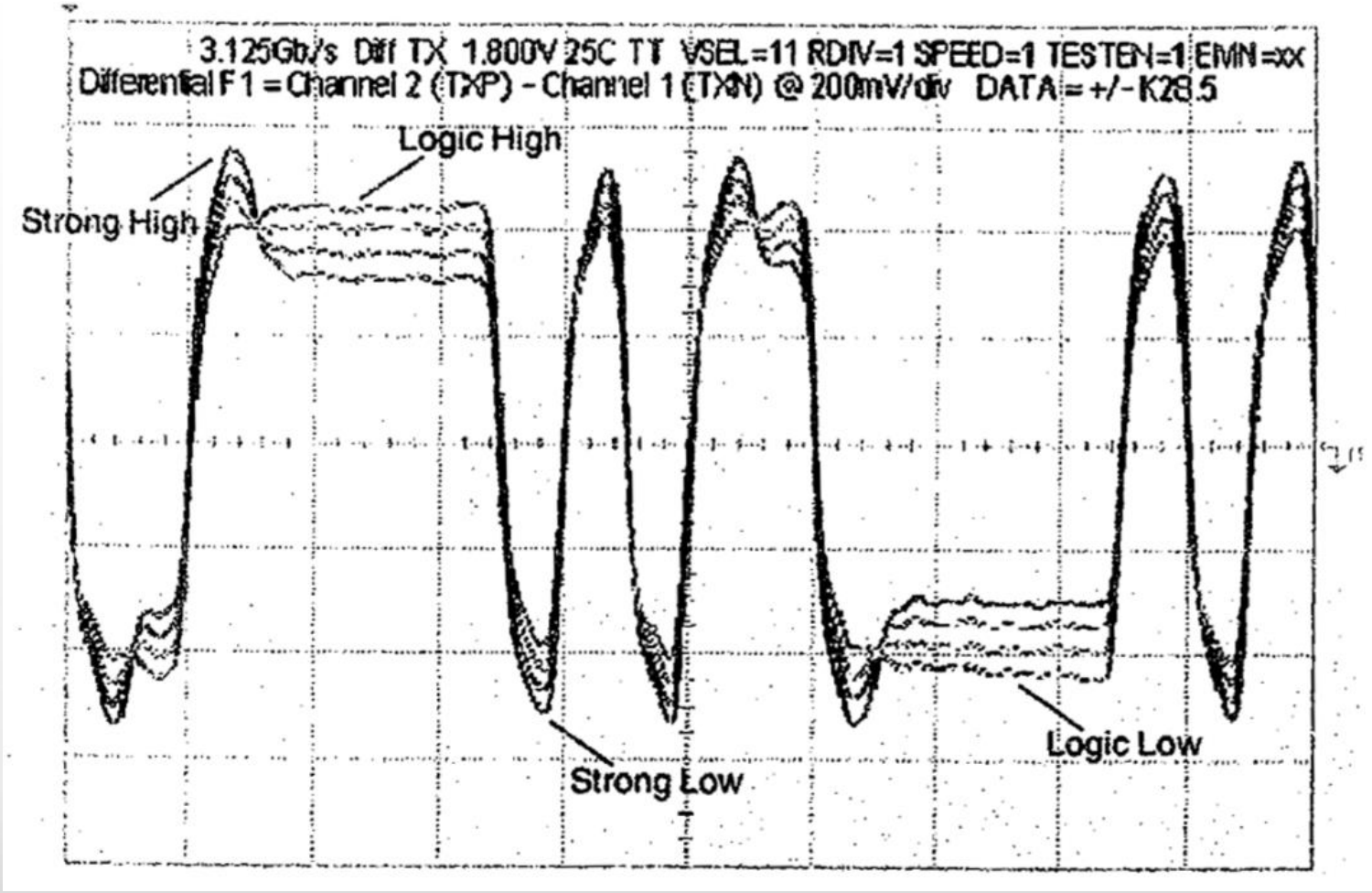
Data Encoder

- Several continuous ‘0’s or ‘1’s will disturb direct current (DC) balance after serialization
- In an 8 to 10 data encoder, series of bits will be encoded in a way that there are no 5 continuous ‘0’s or ‘1’s in the final sequence
- Scrambling is another method for increasing the number of states and error reduction



Picture Source: Computer-Aided Digital Systems Design, Dr Morteza Seheb Zamani, page 94, with modifications

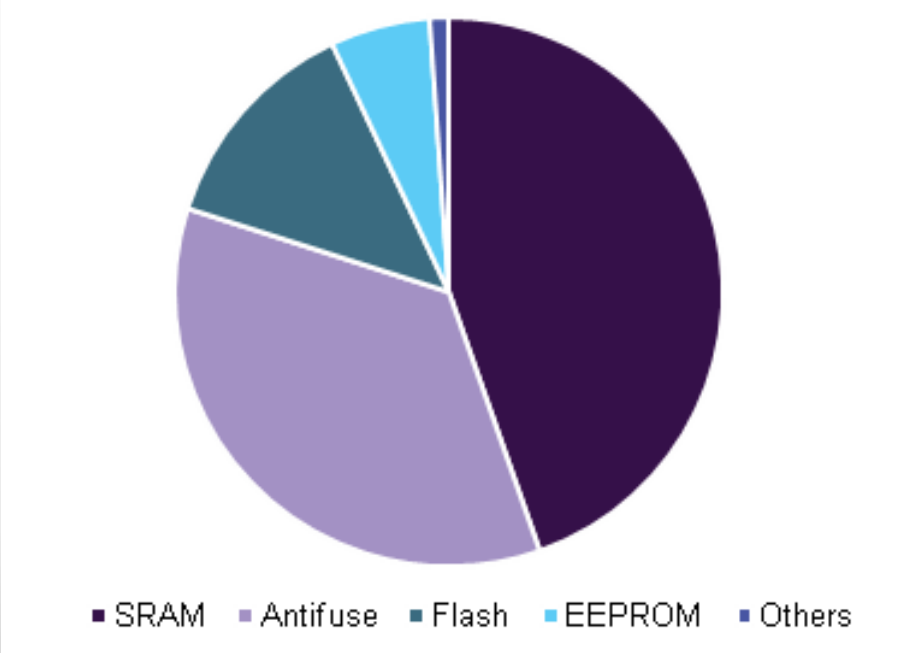
Pre-emphasis



Picture Source: Computer-Aided Digital Systems Design, Dr Morteza Seheb Zamani, page 100

FPLD Programming Technologies

- FPLDs use one of the following technologies for programming:
  - SRAM
  - Flash
  - EEPROM
  - Anti-fuse



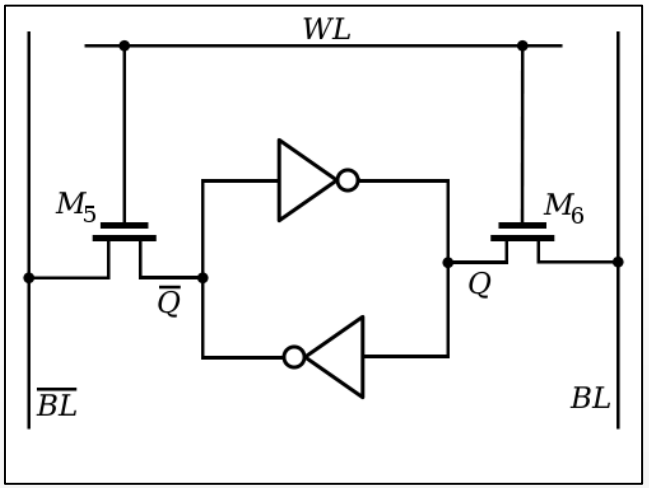
SRAM

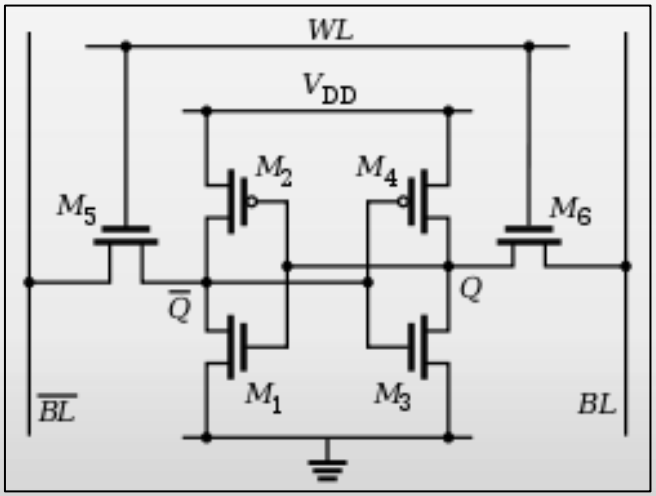
Advantages:

- Unlimited times of programming
- Chip is tested by manufacturer
- Runtime programming

Disadvantages:

- Volatile
- High area
- Low security

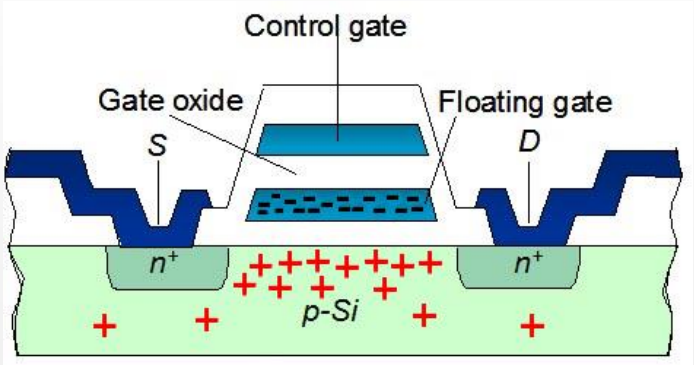




Flash and EEPROM

Advantages:

- Non volatile
- Low area
- High security (due to floating gate tansistors)



Disadvantages:

- High cost of manufacturing (due to FGTs)
- Slower programming compared to SRAM

Flashes and EEPROMs are completely similar; however, in flashes, data is removed in blocks, whereas in EEPROMs it is removed in words.

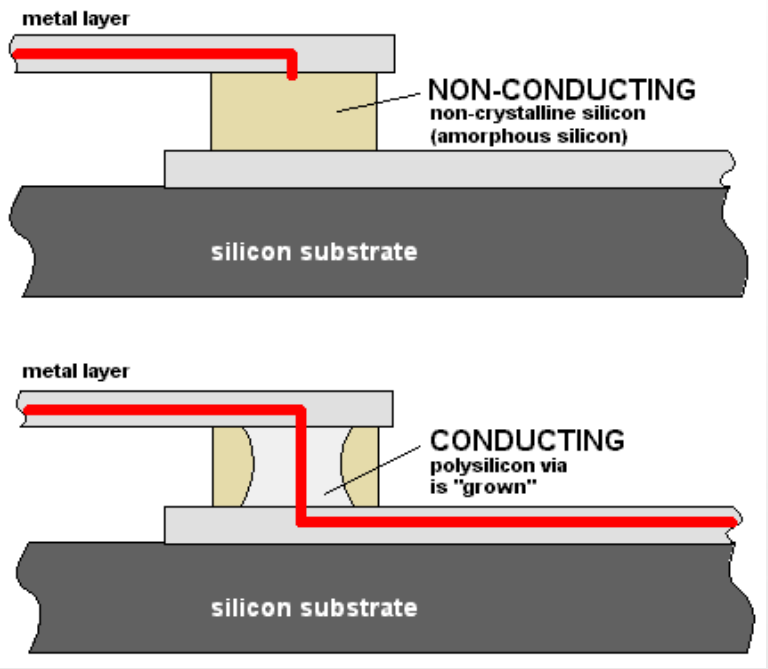
Anit-fuse

Advantages:

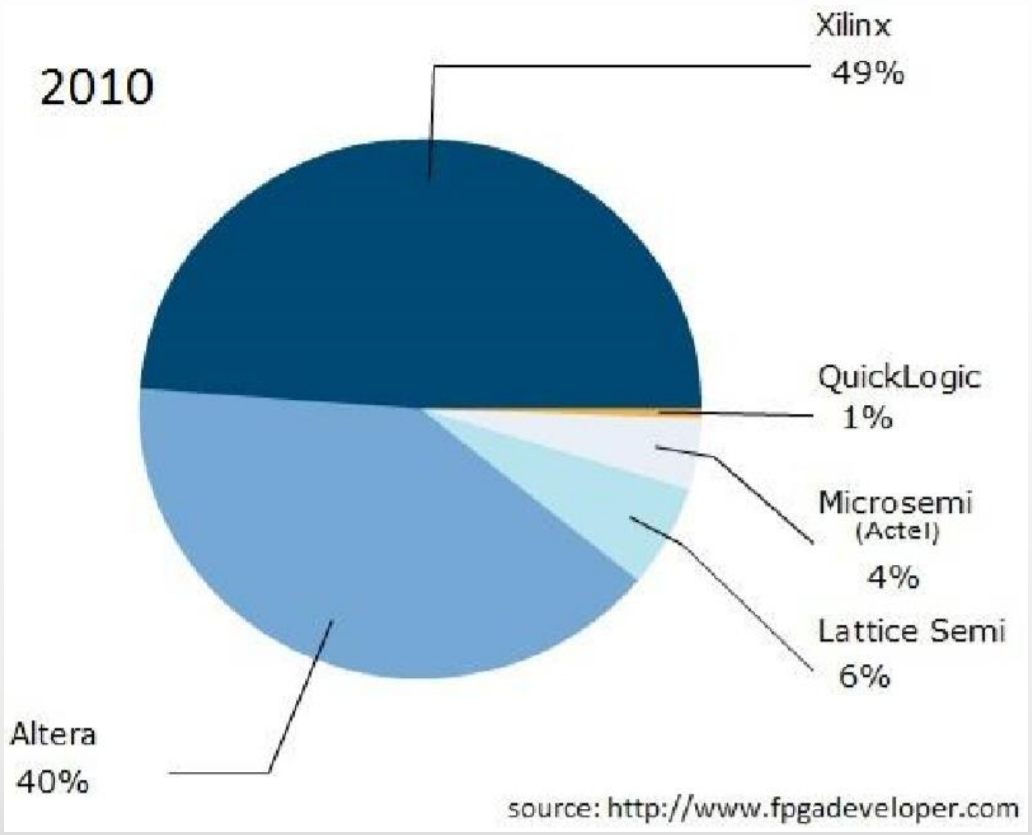
- Non volatile
- Low area
- High security (surgery required for stealing!)
- Low power

Disadvantages:

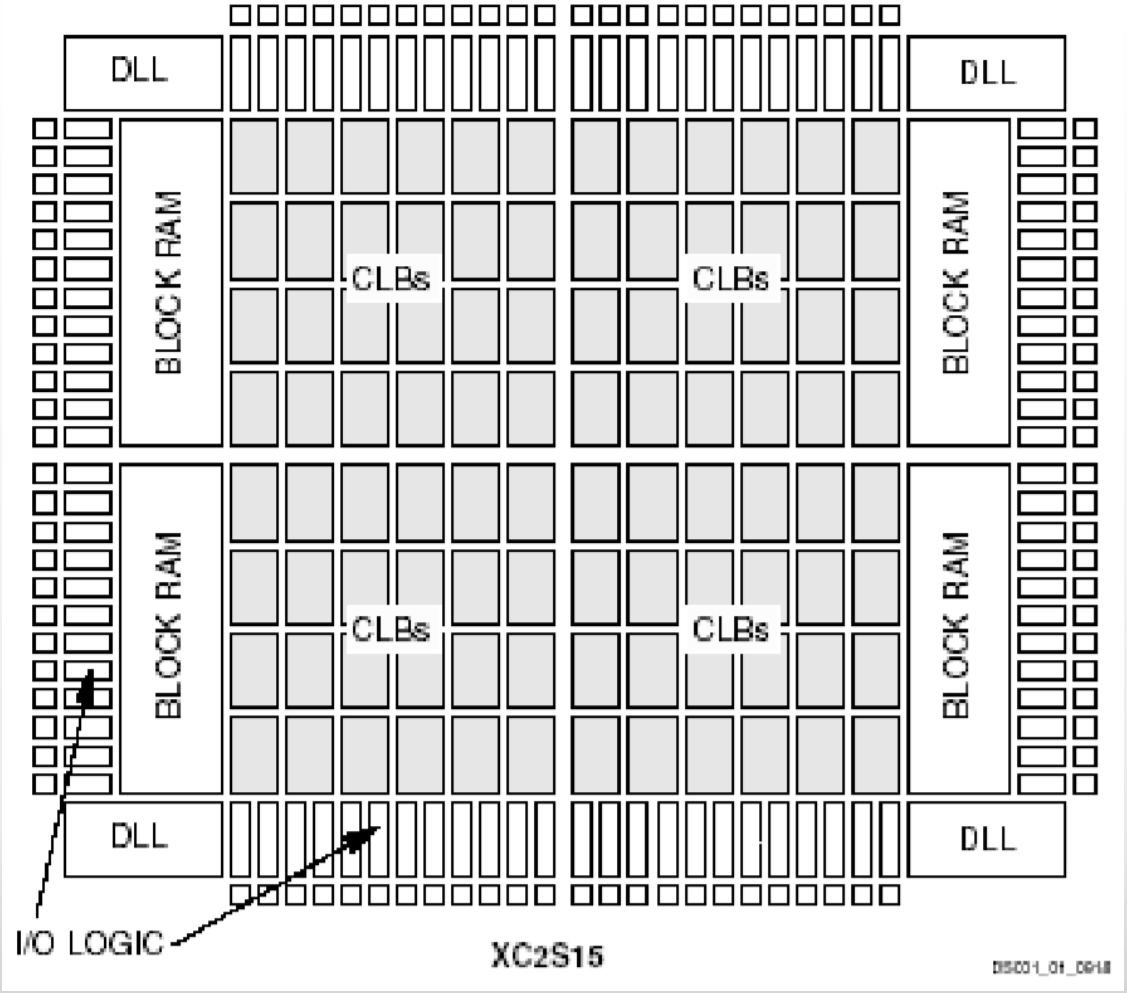
- Not reprogrammable



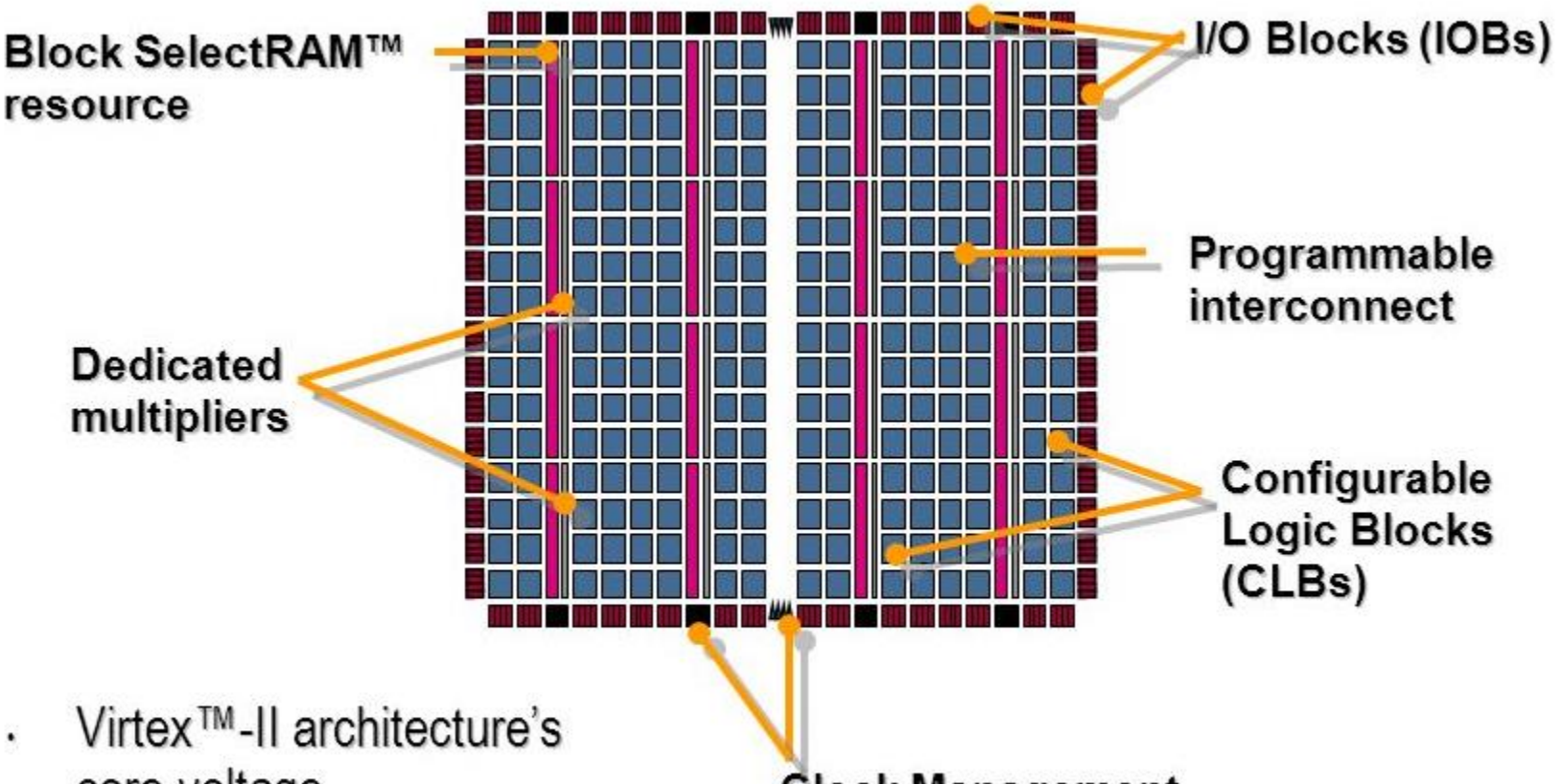
FPGA Market


2010
Xilinx
49%
QuickLogic
1%
Microsemi
(Actel)
4%
Lattice Semi
6%
Altera
40%
source: http://www.fpgadeveloper.com

FPGA Examples: Xilinx Spartan-II

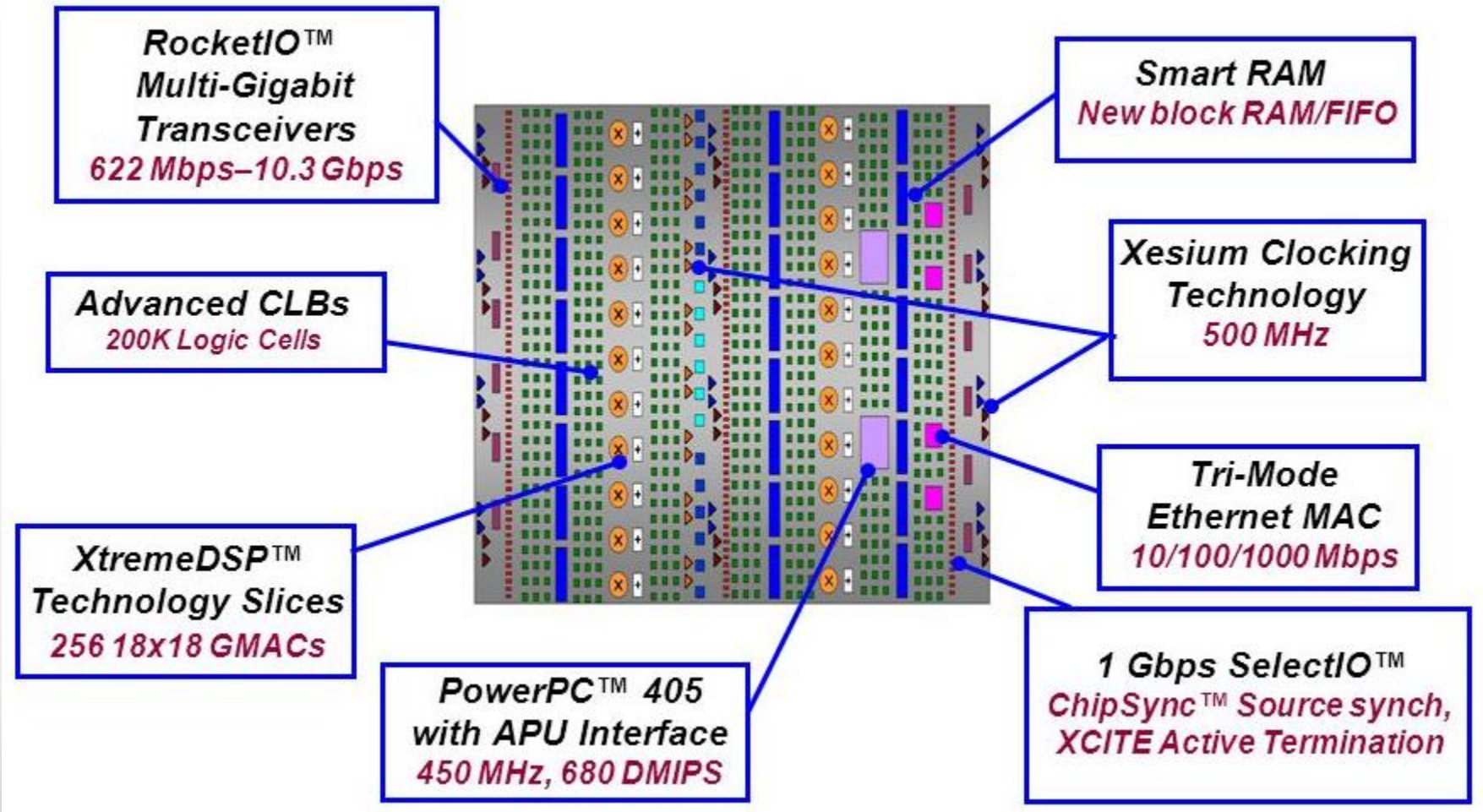


FPGA Examples: Xilinx Virtex-II

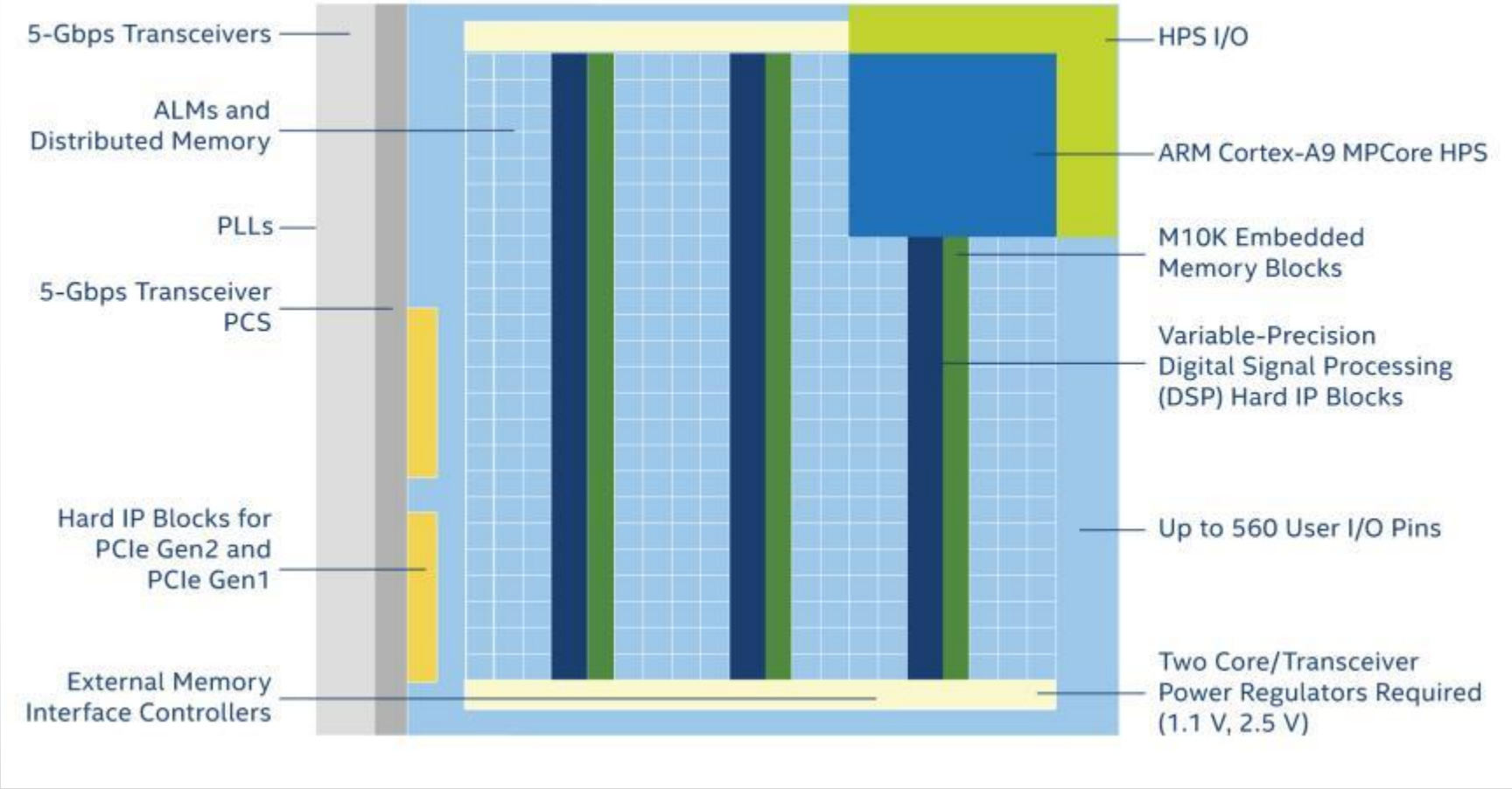


- Virtex™-II architecture's core voltage operates at 1.5V

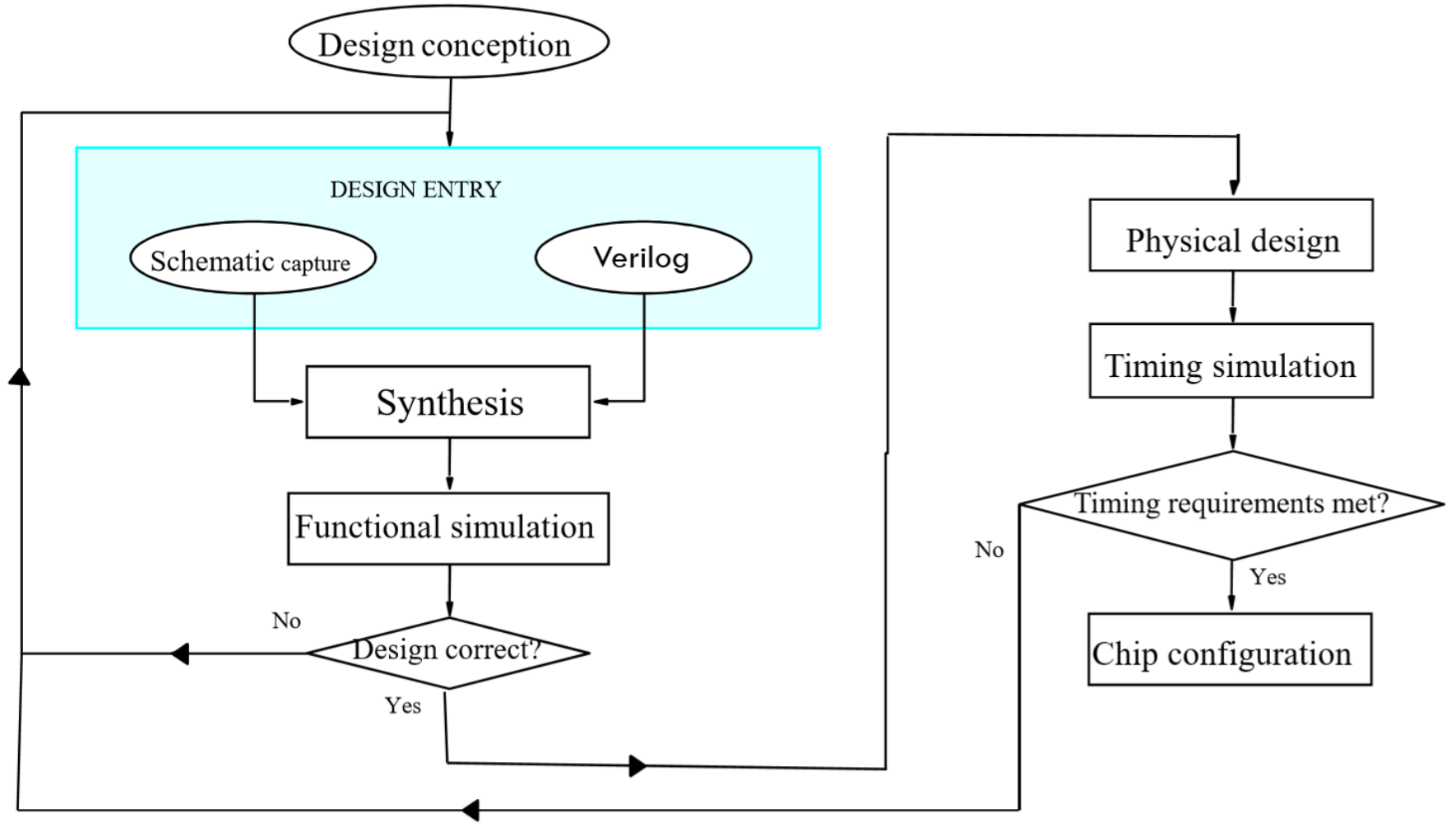
FPGA Examples: Xilinx Virtex-IV



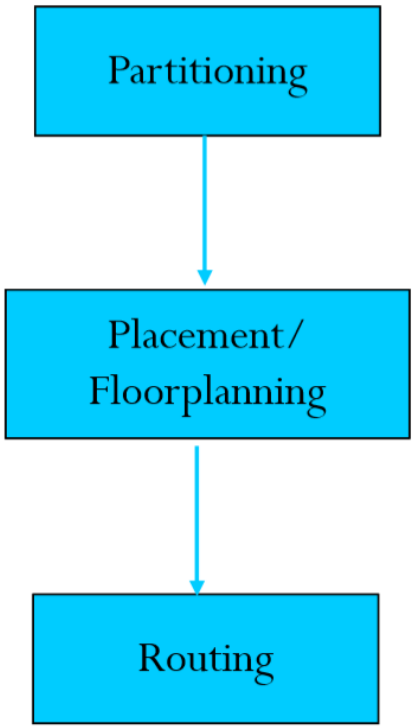
FPGA Examples: Altera Cyclone V

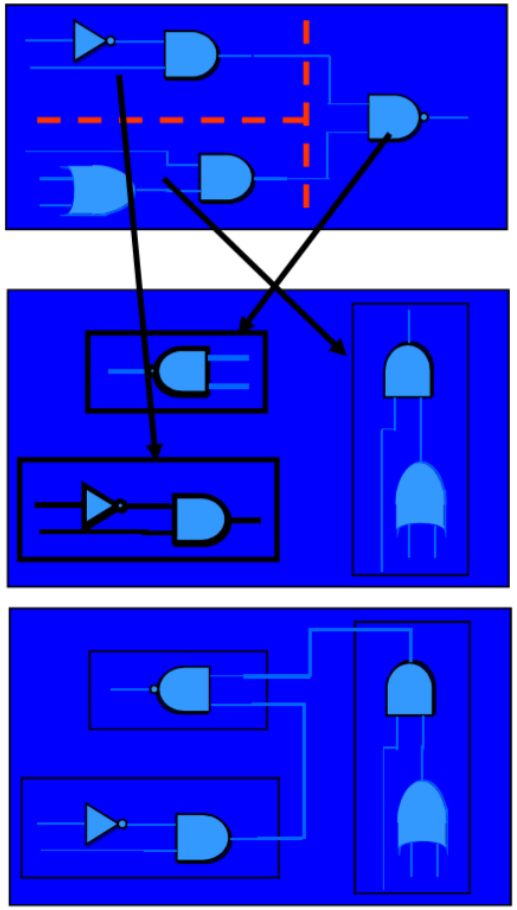


Design Flow


Design conception
DESIGN ENTRY
Schematic capture
Verilog
Synthesis
Functional simulation
No
Design correct?
Yes
Physical design
Timing simulation
Timing requirements met?
No
Yes
Chip configuration

Physical Design





Break the circuit up into smaller segments

Place the segments on the chip

Layout out the wire paths

Picture Source: CEIT483 at Amirkabir U. ofTech., Lecture 2, by Dr Saheb-zamani, with modifications

Further Reading

[1] Computer-Aided Digital Systems Design, Dr Morteza Seheb Zamani
Chapter 1 - 3

Any Question?